

10/039126

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,784,476 B2
DATED : August 31, 2004
INVENTOR(S) : Kim et al.

Page 1 of 6

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page

Title page illustrating figure(s) should be deleted, and substituted therefore, the title page illustrating figure(s). (attached)

Drawings

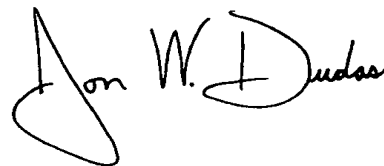
Delete drawing sheets 4, 8, 9 & 19, and substitute therefore, drawing sheets 4, 8, 9 & 19. (attached)

Column 9,

Line 64, delete "gale" and insert -- gate --.

Signed and Sealed this

Fifth Day of April, 2005

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a distinct "D" at the end.

JON W. DUDAS

Director of the United States Patent and Trademark Office

(12) **United States Patent**
Kim et al.

(10) Patent No.: **US 6,784,476 B2**
(45) Date of Patent: **Aug. 31, 2004**

(54) **SEMICONDUCTOR DEVICE HAVING A
FLASH MEMORY CELL AND FABRICATION
METHOD THEREOF**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/039,126**

(22) Filed: **Jan. 3, 2002**

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(30) **Foreign Application Priority Data**

Jan. 31, 2001 (KR) 2001-04588

(51) Int. Cl.⁷ **H01L 27/108; H01L 29/76;
H01L 29/94; H01L 31/119**

(52) U.S. Cl. **257/296; 257/314**

(58) Field of Search **257/296, 311,
257/315, 316, 314, 319, 320, 318, 336,
344, 408, 549, 550**

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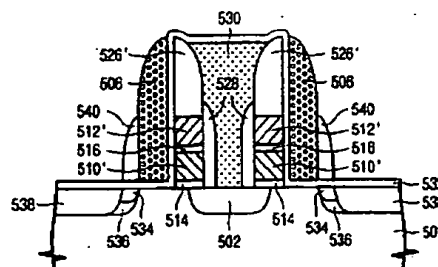
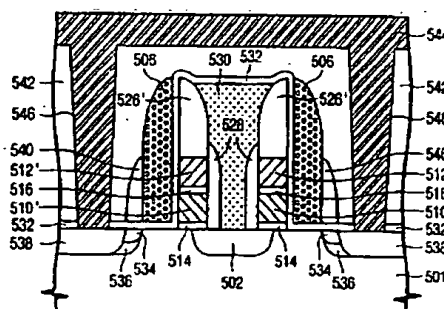
Primary Examiner—David Nhu

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(57) **ABSTRACT**

In a non-volatile semiconductor memory device and a fabrication method thereof, a charge storage layer is formed on a substrate. A control gate layer is formed on the charge storage layer. A gate mask having a spacer-shape is formed on the control gate layer. The charge storage layer and the control gate layer are removed using the gate mask as protection to form a control gate and a charge storage region.

15 Claims, 19 Drawing Sheets

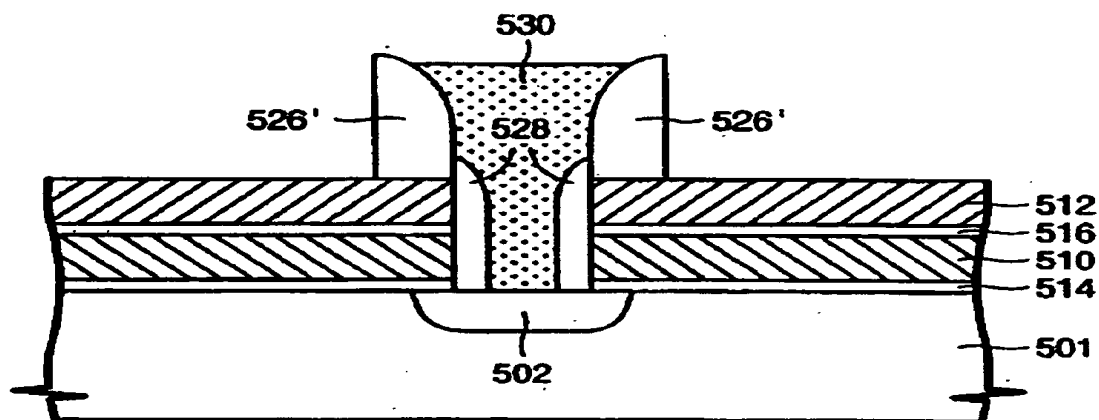
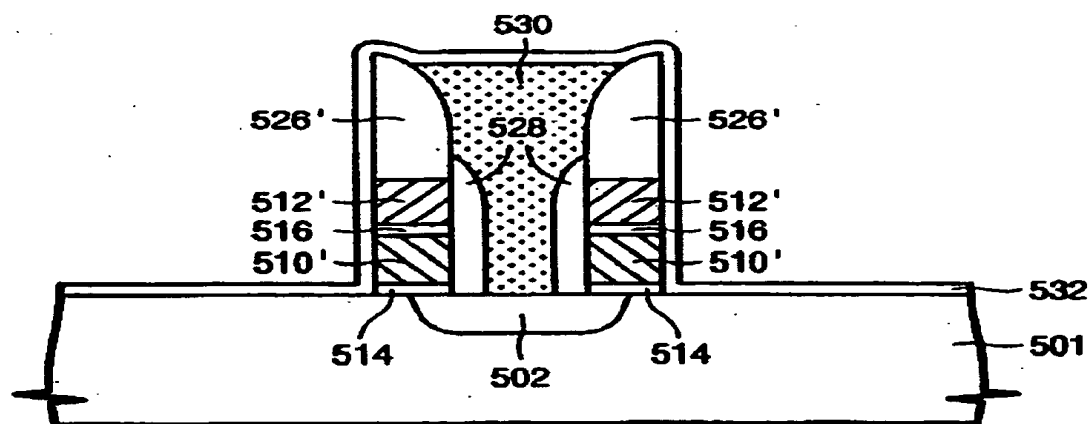


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Fig. 7G**Fig. 7H**

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Fig. 7I

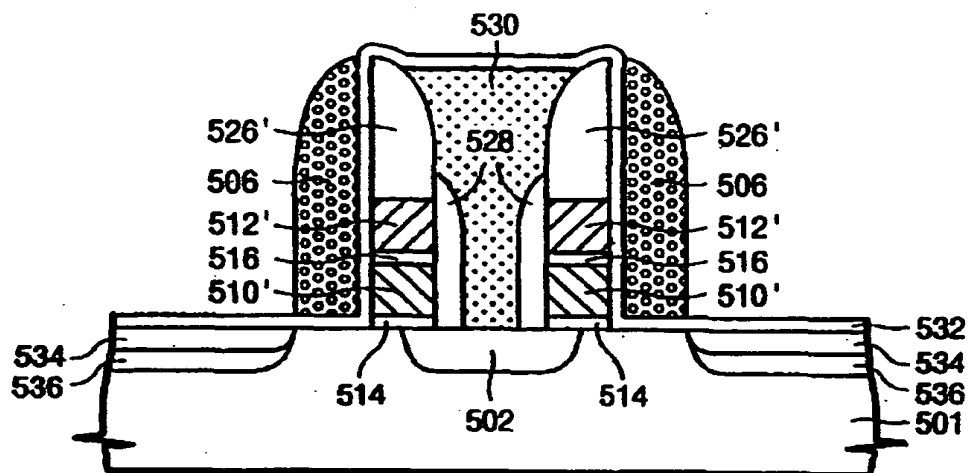
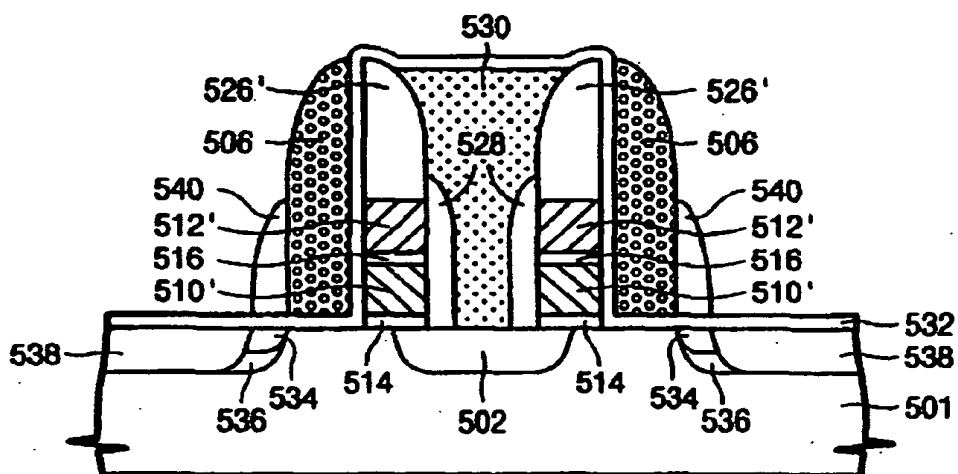


Fig. 7J



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Fig. 9I

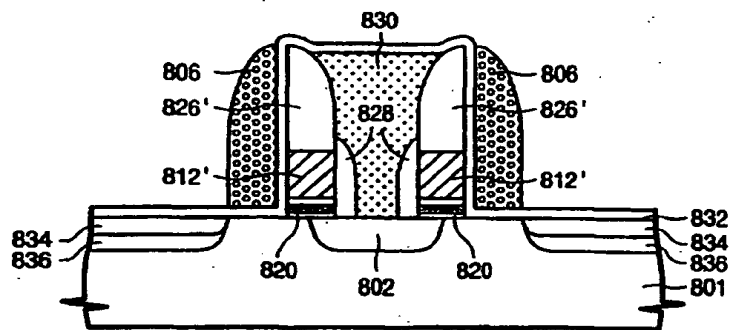


Fig. 9J

